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AMENDMENTS TO THE CLAIMS:

Claim 15. (Original) A method of forming an N-channel metal oxide semiconductor (NMOS) driver circuit, comprising:

forming a boost gate stack on a substrate, said boost gate stack having a source and drain formed by a low concentration N-type implantation; and
coupling an N-driver to said boost gate stack.

Claim 16. (Currently Amended) A method according to claim 15, further comprising:

forming a contacts adjacent sides of said boost gate stack for coupling said boost gate stack to said N-driver.

Claim 17. (Currently Amended) The method according to claim 16, wherein said boost gate stack is ~~formed~~ adjacent to a memory array, said low concentration N-type implantation comprising ~~being~~ a memory array implantation.

Claim 18. (Original) The method according to claim 15, wherein said low concentration N-type implantation improves a reliability of said driver circuit by increasing a junction breakdown voltage and lowering a contact resistance thereof.

Claim 19. (Original) The method according to claim 16, wherein said contacts comprise memory array bitline contacts.

Claim 20. (Currently Amended) The method according to claim 19, wherein said bitline contacts comprise ~~are formed of~~ polysilicon.

Claim 21. (Currently Amended) The method according to claim 20, wherein said bitline contacts comprise ~~are formed of~~ N-type doped polysilicon contacts, and the dopants are annealed and driven into said substrate to reduce the contact resistance.

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Claim 22. (Currently Amended) The according to claim 15, wherein contacts are ~~formed~~ adjacent first and second sides of said boost gate stack.

Claim 23. (Original) The method according to claim 15, wherein said boost gate stack forms a boost device, said boost device having a channel length which is greater than a minimum channel length, said minimum channel length being a lithographically patternable feature size.

Claim 24. (Original) The method of forming an NMOS driver circuit according to claim 15, further comprising:

forming a main wordline driver coupled to a plurality of sub-array drivers, each of said plurality of sub-array drivers coupled to a corresponding boost gate stack.

Claim 25. (Currently Amended) The method according to claim 24, wherein a boost node of ~~said~~ each boost gate stack is connected to a corresponding gate of said sub-array drivers.

Claim 26. (Original) The method according to claim 25, wherein a distance from an edge of said low concentration N-type implantation to an N diffusion area of a device junction is a minimum ground rule, and

wherein a distance from an edge of said low concentration N-type implantation to an edge of an adjacent pull-up device is also a minimum ground rule.

Claim 27. (Original) The method according to claim 15, wherein said contacts comprise doped polysilicon contacts, and wherein said doped polysilicon contacts and said source and drain are self-aligned to the boost gate stack.

Claim 28. (Currently Amended) The method according to claim 21, wherein said doped polysilicon contacts form ~~forms~~ a self-aligned junction with said boost gate stack.

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Claim 29. (Currently Amended) A The method of forming an N-channel metal oxide semiconductor (NMOS) driver circuit, comprising:

- forming a boost gate stack on a substrate adjacent to a memory array;
- using a low-concentration N-type implantation to form a source and drain in said substrate for said boost gate stack; and
- coupling an N-driver to said boost gate stack.

Claim 30. (Original) The method according to claim 29, further comprising:

- forming contacts adjacent said gate stack.

Claim 31. (Original) A method of fabricating an N-channel metal oxide semiconductor (NMOS) driver circuit, comprising:

- forming a shallow trench isolation (STI) and a gate on a substrate, said gate forming a portion of a boost device for the driver circuit;

- forming a source and a drain for said boost device by a low concentration N-type implantation;

- depositing a layer of dielectric adjacent said boost device;

- patterning said dielectric layer;

- forming contacts in said patterned area of said dielectric layer;

- annealing said contacts; and

- connecting a boost node of said boost device to a gate of a sub-array device.

Claim 32. (Original) The method as claims in claim 31, wherein said sub-array device is adjacent to and contacts said boost device.

Claim 33. (Currently Amended) A method as claims in claim 31, wherein said contacts comprise ~~are formed in a~~ self-aligned contacts ~~manner~~.

Claim 34. (Original) The method as claims in claim 31, wherein said boost device has a

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channel length which is greater than a minimum channel length as determined by a design rule.

Claim 35. (Original) The method as claimed in claim 32, wherein said sub-array device has a channel length which is greater than a minimum channel length as determined by a design rule.

Claim 36. (Original) The method as claimed in claim 31, wherein a node of said boost device is connected to a gate of said sub-array device.

Please add the following new claims:

Claim 37. (New) The method according to claim 15, wherein said low concentration N-type implantation comprises no more than about 1×10^{14} dopant ions per cm^3 .

Claim 38. (New) The method according to claim 15, wherein said low concentration N-type implantation comprises about 1×10^{13} dopant ions per cm^3 to 1×10^{14} dopant ions per cm^3 .

Claim 39. (New) The method according to claim 15, wherein said low concentration N-type implantation comprises one of phosphorus ions and boron ions.